CLAIMS

1. A method for filling a line in a cache, comprising the steps of:

sending a request for data to be provided on a data bus to the cache at a first address;

sending a first request external to the cache for first data at the first address;

sending for additional data at additional addresses, the additional addresses being consecutive with the first address;

receiving the first data located at the first address;

placing the first data in the line in the cache and onto the data bus;

loading the additional data into the line in the cache as it is received;

terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses; and

sending the second request external to the cache for the different data at the different address.

2. The method of claim 1, further comprising:

continuing loading the additional data into the line in the cache as it is received in response to receiving a data request at one of the additional addresses for data not present in the cache.

3. A method for operating a processing system comprising a cache and a processor, comprising the steps of:

generating a first request for data from the cache at a fetch address;

providing the fetch address for a memory that is outside of the cache if there is a miss in the cache;

continuously providing prefetch addresses consecutive with the fetch address for the memory;

generating a second request for data that is different from the prefetch addresses that have been provided;

terminating the providing of prefetch addresses in response to the second request.

4. The method of claim 3, further comprising:

loading the data from the first request in a line in the cache;

loading data corresponding to the prefetch addresses in the line in the cache; and

terminating the loading of the data corresponding to the prefetch addresses in response to the second request.

5. The method of claim 4, further comprising:

generating a third request for data that is not in the cache, prior to the second request for data, that is one of the prefetch addresses; and

continuing loading data corresponding to the prefetch addresses in the line in the cache in response to the third request.

6. A processing system, comprising:

a processor for generating data requests at address locations from an external memory that is external to the processing system;

a cache, coupled to the processor, for storing data corresponding to at least some of the address locations;

fetch means, coupled to the cache and the processor, for providing a fetch address for the external memory in response to a request from the processor that results in a miss in the cache, providing requests for the external memory for data at additional addresses that are consecutive with the fetch address in response to receiving the request for the fetch address, and terminating the requests for the additional addresses in response to receiving a data request from the processor for data at an address that is different from any of the additional addresses.

7. The processing system of claim 6, wherein the fetch means is further characterized as not terminating the requests for additional requests for the additional addresses in response to receiving a data request from the processor for data at one of the additional addresses that is a miss in the cache.

8. The processing system of claim 7, wherein the cache is characterized as having plurality of lines that each comprise locations having consecutive addresses, and wherein the additional addresses requested by the fetch means are for locations in the cache that are in a line in the plurality of lines.

9. The processing system of claim 8, further comprising system interface means coupled between the fetch means and the external memory.

10. A processing system comprising::

a cache for storing data and providing a hit signal if a request for data is contained in the cache and a miss signal if the request for data is not contained in the cache;

processor means, coupled to the cached, for sending a request for data to the cache at a first address;

fetch means, coupled to the cache and the processor means, for sending the request external to the cache for first data at a first address in response to the miss signal, sending for additional data at additional addresses, the additional addresses being consecutive with the first address, receiving the first data located at the first address, placing the first data in the cache and onto the data bus, loading the additional data into the line as it is received, and terminating the loading of the additional data in response to a second request for different data that is at a different address from the additional addresses.

11. The processing system of claim 10, wherein the fetch means is further characterized as sending the second request external to the cache for the different data at the different address.

12. The processing system of claim 11, wherein the cached is characterized as having plurality of lines that each comprise locations having consecutive addresses, and wherein the additional addresses requested by the fetch means are for locations in the cache that are in a line in the plurality of lines.

13. The processing system of claim 12, further comprising a system interface coupled to the fetch for interfacing between the fetch means and an external memory.

14. The processing unit of claim 10 wherein the fetch means is further characterized as continuing loading the additional data if a third request is received from the processor means that is a miss in the cache and is for one of the additional addresses.